WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a memory cell array in which memory cells each of which stores information by using a magneto-resistive effect are arranged in a matrix;

a constant current circuit which is connected to a first potential supply source and used to write data in each memory cell in the memory cell array; and

a current peak suppressing circuit configured to suppress a current peak that is generated at a write start timing due to charges which flow out from a parasitic capacitance connected to an output terminal of the constant current circuit or charges which flow into the parasitic capacitance, the current peak suppressing circuit having switch circuits to selectively supply an output from the constant current circuit to a specific write line, and a circuit portion which connects one of two terminals of each of the switch circuits to a second potential supply source having a potential different from that of the first potential supply source before the timing of the start of the write operation and short-circuits the two terminals of each of the switch circuits immediately after the start of the write operation.

2. A device according to claim 1, wherein the

current peak suppressing circuit is connected to each write line.

3. A device according to claim 2, wherein the current peak suppressing circuit is a current sink connected to each write line.

4. A device according to claim 3, wherein the constant current circuit is a current source and is shared by at least two current sinks.

5. A device according to claim 3, wherein each write line is set to a ground potential by the current sink in a standby mode.

6. A device according to claim 2, wherein the current peak suppressing circuit is a current source connected to each write line.

7. A device according to claim 6, wherein the constant current circuit is a current sink and is shared by at least two current sources.

8. A device according to claim 7, wherein each write line is set to a power supply potential by the current source in a standby mode.

9. A device according to claim 2, wherein there exists a period during which both a switch element of the switch circuit, which is connected to a write line connected to a memory cell to be write-accessed, and an element that constitutes the current peak suppressing circuit are set in an ON state at the start of the write operation.

10. A device according to claim 1, wherein the current peak suppressing circuit are separated, through a dedicated switch element, from the switch circuits connected to the write lines.

11. A device according to claim 10, wherein the current peak suppressing circuit is a current sink shared by a plurality of write lines.

12. A device according to claim 11, wherein the constant current circuit is a current source and is shared by at least two write lines.

13. A device according to claim 12, wherein each write line is set to a ground potential by the current sink in a standby mode.

14. A device according to claim 10, wherein the current peak suppressing circuit is a current source connected to each write line.

15. A device according to claim 14, wherein the constant current circuit is a current sink and is shared by at least two write lines.

16. A device according to claim 15, wherein each write line is set to a power supply potential by the current source in a standby mode.

17. A device according to claim 10, wherein the dedicated switch element to separate the current peak suppressing circuit from the switch circuits connected to the write lines is exclusively ON/OFF-controlled so as to or not to be electrically connected to the

current peak suppressing circuit.

18. A semiconductor integrated circuit device comprising:

a plurality of memory cell blocks in which memory cells each of which stores information by using a magneto-resistive effect are arranged in a matrix;

a constant current circuit which is used to write data in each memory cell in the memory cell blocks, the constant current circuit being shared by two adjacent memory cell blocks;

switch circuits which are arranged in correspondence with each memory cell block and configured to selectively connect an output from the constant current circuit to a specific write line; and

a current peak suppressing circuit configured to suppress a current peak at a timing of a start of a write operation.

19. A semiconductor integrated circuit device comprising:

a plurality of memory cell blocks in which memory cells each of which stores information by using a magneto-resistive effect are arranged in a matrix;

a constant current circuit which is used to write data in each memory cell in the memory cell blocks;

switch circuits which are arranged in correspondence with each memory cell block and configured to selectively connect an output from the

constant current circuit to a specific write line; and

a current peak suppressing circuit configured to suppress a current peak at a timing of a start of a write operation,

wherein the constant current circuit and the current peak suppressing circuit are shared by two adjacent memory cell blocks.

20. A semiconductor integrated circuit device comprising:

write lines to write information in memory cells each of which stores information by using a magneto-resistive effect;

a constant current circuit which is connected to a first potential supply source and used to write data in the memory cells;

switch circuits each having one terminal connected to a corresponding one of the write lines and the other terminal connected to an output terminal of the constant current circuit in parallel; and

a current peak suppressing circuit which has a circuit portion to which said one terminal of each of the switch circuits is connected and is configured to connect one of the two terminals of each of the switch circuits to a second potential supply source having a potential different from that of the first potential supply source before a timing of a start of a write operation and short-circuit the two terminals of each

of the switch circuits immediately after the start of the write operation.